AMENDMENTS TO THE CLAIMS

Please cancel Claims 2 and 18 without prejudice. Please amend the remaining claims according to the following listing. This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS

1. (Currently Amended) A runtime repairable processor within a single silicon chip, comprising:

a plurality of data paths that are contained on a first area on the silicon chip;

a plurality of data registers disposed on the silicon chip and coupled to the plurality of data paths;

a first ~~computing~~ functional unit disposed on the first area of the silicon chip and coupled to the plurality of data paths;

a second area on the silicon chip that is a portion of the first area and smaller that the first are, the second area incapable of receiving thereon a functional unit that would require a data path that is different from the plurality of data paths;

~~an area of the silicon chip defined by at most a plurality of data paths for connecting the plurality of data registers to the first computing unit; and~~

a second ~~computing~~ functional unit that is a duplicate of the first functional unit and that is disposed on the second area of the silicon chip, the second functional unit coupled to the plurality of data paths; and

an enabling control logic that is configured to disable the first functional unit and to enable the second functional unit when a failure is detected with the first functional unit.

~~, wherein the second computing unit is a duplicate of the first computing unit and is connected to the plurality of data registers, the first computing unit and the second computing unit being~~

~~placed within the area.~~

2. (Cancelled)

3. (Currently Amended) The runtime repairable processor of claim ~~2~~ 1, wherein the enabling control logic enables the second functional unit ~~a computing unit~~ by enabling a clock signal to the second functional unit. ~~that computing unit.~~

4. (Currently Amended) The runtime repairable processor of claim ~~2~~ 1, further comprising a machine state register including a unit selecting indicator, the unit selecting indicator configured to control ~~controlling~~ the enabling control logic.

5. (Original) The runtime repairable processor of claim 4, wherein the unit selecting indicator is set by software.

6. (Currently Amended) The runtime repairable processor of claim 1, wherein the first functional ~~computing~~ unit further comprises a first error indicator and the second functional ~~computing~~ unit further comprises a second error indicator.

7. (Currently Amended) The runtime repairable processor of claim 6, further comprising a machine check trap wherein the first error indicator and the second error indicator ~~indicators~~ are stored, the machine check trap ~~being used~~ configured to initiate a software diagnostic routine.

8. (Currently Amended) The runtime repairable processor of claim 1, wherein the first functional ~~computing~~ unit is an adder.

9. (Currently Amended) The runtime repairable processor of claim 1, wherein the first functional ~~computing~~ unit is a rotator.

10. (Currently Amended) The runtime repairable processor of claim 1, wherein the first functional ~~computing~~ unit is an arithmetic logic unit.

11. (Currently Amended) A method for providing a fault tolerant computing ~~through a single chip~~ runtime repairable processor on a single silicon chip, comprising the steps of:

connecting a plurality of data registers to a first functional ~~computing~~ unit through a plurality of data paths, the plurality of data paths that are contained on a first area of the silicon chip, the plurality of data registers and the first functional unit disposed on the first area of the silicon chip;

~~defining an area of the chip that covers at most the plurality of the data paths, wherein the first computing unit and the plurality of data registers are confined within the area;~~

placing a second functional ~~computing~~ unit, that is a duplicate of the first functional unit, on a second area on the silicon chip that is a portion of the first area and that is smaller than and included in the first area, wherein the second area is incapable of receiving thereon a functional unit that would require a data path that is different from the plurality of data paths; ~~within the area, wherein the second computing unit being a duplicate of the first computing unit~~;

connecting the plurality of data registers to the second functional ~~computing~~ unit through the plurality of data paths;

detecting an error condition in the first functional ~~computing~~ unit;

in response to detecting the error condition, disabling the first functional ~~computing~~ unit~~; and~~

~~in response to disabling the first computing unit,~~ enabling the second functional ~~computing~~ unit.

12. (Original) The method of claim 11, wherein the disabling step and the enabling step are controlled by a machine state register.

13. (Original) The method of claim 11, further comprising the step of, in response to detecting an error condition, setting a unit swapping indicator in a machine state register.

14. (Original) The method of claim 11, further comprising the step of, in response to detecting an error condition, executing a diagnostic procedure.

15. (Currently Amended) The method of claim 11, wherein the step of disabling the first functional ~~computing~~ unit further comprises the step of disabling a clock signal to the first functional ~~computing~~ unit.

16. (Currently Amended) The method of claim 11, wherein the step of enabling the second functional ~~computing~~ unit further comprises the step of enabling a clock signal to the second functional ~~computing~~ unit.

17. (Currently Amended) The method of claim 11, further comprising the steps of:
trapping the error condition in a machine check trap; and
in response to trapping the error condition, causing a diagnostic routine to run on the first functional ~~computing~~ unit.

18. (Canceled)